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Clean Version of Pending Claims

CHEMICAL VAPOR DEPOSITION OF TITANIUM

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Claims 46-47 and 57-82, as of February 18, 2003 (date response to final office action filed).

46. A memory, comprising:
a memory array;
a control circuit, operatively coupled to the memory array;
an I/O circuit, operatively coupled to the memory array; and
wherein the memory array, control circuit and I/O circuit each comprise:
a layer of a titanium alloy, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and
a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the layer.
47. The memory of claim 46, wherein the titanium alloy comprises titanium and zinc.
57. A memory device, comprising:
a memory array;
a control circuit operatively coupled to the memory array; and
an I/O circuit operatively coupled to the memory array;
wherein at least one of the memory array, control circuit and I/O circuit comprises a contact having a titanium alloy layer formed overlying walls of a contact hole and a titanium silicide layer formed overlying an exposed silicon base layer of the contact hole, the titanium silicide layer being directly coupled to the titanium alloy layer, and having a composition that is different from the titanium alloy layer.

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58. A memory device, comprising:
a memory array;
a control circuit operatively coupled to the memory array; and
an I/O circuit operatively coupled to the memory array;
wherein at least one of the memory array, control circuit and I/O circuit comprises a via
having a titanium alloy layer formed overlying walls and an exposed base layer of
a contact hole and a fill coupled to the titanium alloy layer, wherein the fill
comprises a metal selected from the group consisting of tungsten and aluminum.
59. (Amended) A memory device, comprising:
a memory array;
a control circuit operatively coupled to the memory array; and
an I/O circuit operatively coupled to the memory array;
wherein at least one of the memory array, control circuit and I/O circuit comprises
a titanium alloy layer formed on overlying walls of a contact opening, wherein the titanium alloy
layer is produced using a method, the method comprising:
forming a seed layer within the contact opening by combining a first
precursor with a first reducing agent; and
forming the titanium alloy layer within the contact opening by combining a
titanium-containing precursor with the seed layer.
60. A memory device, comprising:
a semiconductor substrate;
a memory array coupled to the semiconductor substrate;
a control circuit, operatively coupled to the memory array;
an I/O circuit, operatively coupled to the memory array;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy within a contact opening in the insulating layer, the contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.

61. The memory device of claim 60, wherein the titanium alloy includes titanium and zinc.

62. The memory device of claim 60, wherein the insulator layer includes silicon dioxide (SiO₂).

63. The memory device of claim 60, wherein the electronic device includes a transistor.

64. A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

a transistor formed on the semiconductor substrate, the transistor having a source/drain region;

an insulating layer over the source/drain region;

an alloy layer of a titanium alloy within a contact opening in the insulating layer, the

contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and
a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.

65. The memory device of claim 64, wherein the titanium alloy includes titanium and zinc.
66. The memory device of claim 64, wherein the insulator layer includes silicon dioxide (SiO₂).
67. The memory device of claim 64, wherein the contact opening includes a high aspect ratio contact opening.
68. A memory device, comprising:
a semiconductor substrate;
a memory array coupled to the semiconductor substrate;
a control circuit, operatively coupled to the memory array;
an I/O circuit, operatively coupled to the memory array;
an electronic device formed on the semiconductor substrate, the electronic device having an active region;
a borophosphosilicate glass (BPSG) layer over the active region;
an alloy layer of a titanium alloy within a contact opening in the borophosphosilicate glass (BPSG) layer, the contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium,

tin, silicon, germanium, lead, arsenic and antimony; and
a titanium silicide contact having a composition that is different from the layer of
titanium alloy, the contact being directly coupled to the alloy layer.

69. The memory device of claim 68, wherein the titanium alloy includes titanium and zinc.

70. The memory device of claim 68, wherein the electronic device includes a transistor.

71. The memory device of claim 68, wherein the contact opening includes a high aspect ratio
contact opening.

72. A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

an electronic device coupled to the semiconductor substrate, the electronic device having
an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy within a high aspect ratio contact opening in the

insulating layer, the high aspect ratio contact opening being at least partially over

the active region, wherein the titanium alloy comprises titanium and an element

selected from the group consisting of zinc, cadmium, mercury, aluminum,

gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of
titanium alloy, the contact being directly coupled to the alloy layer.

73. The memory device of claim 72, wherein the titanium alloy includes titanium and zinc.
74. The memory device of claim 72, wherein the electronic device includes a transistor.
75. The memory device of claim 72, wherein the insulator layer includes silicon dioxide (SiO₂).
76. The memory device of claim 72, wherein the insulator layer includes borophosphosilicate glass (BPSG).
77. A memory device, comprising:
a semiconductor substrate;
a memory array coupled to the semiconductor substrate;
a control circuit, operatively coupled to the memory array;
an I/O circuit, operatively coupled to the memory array;
a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;
an insulating layer over the source/drain region;
an alloy layer of a titanium alloy within a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and
a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.

78. The memory device of claim 77, wherein the titanium alloy includes titanium and zinc.
79. The memory device of claim 77, wherein the insulator layer includes silicon dioxide (SiO_2).
80. The memory device of claim 77, wherein the insulator layer includes borophosphosilicate glass (BPSG).
81. A memory device, comprising:
a semiconductor substrate;
a memory array coupled to the semiconductor substrate;
a control circuit, operatively coupled to the memory array;
an I/O circuit, operatively coupled to the memory array;
a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;
a borophosphosilicate glass (BPSG) layer over the source/drain region;
an alloy layer of a titanium alloy within a high aspect ratio contact opening in the borophosphosilicate glass (BPSG) layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and
a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.
82. The memory device of claim 81, wherein the titanium alloy includes titanium and zinc.